AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system, comprising:

a first application specific integrated circuit;

a first random access memory coupled with the first application specific integrated circuit;

a first memory testing engine to execute test operations on the first random access memory;

a first bus slave controller ~~coupled with the first memory testing engine to provide access to the first random access memory~~;

a processor ~~to control the first bus slave controller~~; and

a bus to connect the processor to the first bus slave controller wherein the first bus slave controller is to provide the processor access to the first random access memory, and the processor is to control the first memory testing engine via the bus and the first bus slave controller.

a3

2. (Currently Amended) The system of claim 1, further comprising:

a second application specific integrated circuit;

a second random access memory coupled with the second application specific integrated circuit;

a second memory testing engine to execute test operations on the second random access memory~~, the second memory testing engine controlled by the processor via the bus~~; and

a second bus slave controller connected to the processor by the bus, wherein the second bus slave controller is ~~coupled with the second memory testing engine~~ to provide the processor access to the second random access memory, and the processor is to control the second memory testing engine via the bus and the second bus slave controller.

3. (Currently Amended) The system of claim 2, wherein the first and second memory testing ~~engine~~ engines can perform testing operations concurrently.

4. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine is integrated with the ~~slave~~ first bus slave controller.

5. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine generates test data and expected responses.

6. (Currently Amended) The system of claim 5, wherein the first memory ~~test~~ testing engine captures and compares an actual random access memory response to the test data.

7. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine is responsible for programmable address ranges and data widths.

8. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine ~~tests memory in an incrementing memory address order~~uses data, address and control pathways used by the first bus slave controller so that if data traffic is being passed to a memory module by the first bus slave controller, the first memory testing engine cannot run a test function.

a3

9. (Currently Amended) The system of claim 1 further comprising a register controller for the processor to configure the first memory testing engine, ~~wherein the memory test engine tests memory in a decrementing memory address order~~and a memory controller for accessing the first random access memory.

Claims 10-11 (Canceled).

12. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine saves a failing address for the processor.

13. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine saves a failing data value for the processor.

14. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine discontinues an active test until the processor reads a failing address and a memory address location.

15. (Currently Amended) The system of claim 1, wherein the first memory ~~test~~ testing engine reports an asynchronous interrupt to the processor.

16. (Currently Amended) A method, comprising:

transmitting ~~an initiation signal~~a plurality of initiation signals from a processor via a bus to a ~~first~~ plurality of memory testing ~~engine~~ engines ~~coupled with a first application specific integrate circuit~~ via a ~~first~~ plurality of bus slave ~~controller~~controllers, respectively; ~~and~~

testing ~~a first random access memory associated with the first integrated circuit~~a plurality of random access memories that are associated with a plurality of ASICs, respectively, using the ~~first~~ plurality of initiated memory testing ~~engine~~engines, respectively; and

accessing from the processor the plurality of random access memories via the plurality of bus slave controllers, respectively.

a3

17. Canceled.

18. (Currently Amended) The method of claim ~~17~~16, wherein testing by the plurality of memory testing engines is concurrent.

19. (Original) The method of claim 16, further comprising generating test data and expected responses.

20. (Original) The method of claim 19, further comprising capturing and comparing an actual random access memory response to the test data.

21. (Currently Amended) The method of claim 16, wherein testing comprises writing multiple data patterns per ~~a~~ memory location within ~~the first~~a random access memory and comparing a reading of the location with an expected response.

22. (Currently Amended) The method of claim 16, further comprising ~~testing memory in an incrementing memory address order~~passing control of data, address and control pathways between (1) each one of the memory test engines, and (2) a respective one of the bus slave controllers, so that only one of the two has control at one time.

23. (Currently Amended) The method of claim 16, further comprising ~~testing memory in a decrementing memory address order~~:

accessing from the bus slave controllers the random access memories using a plurality of memory controllers, respectively; and

configuring the memory test engines using a plurality of register controllers, respectively.

Claims 24-25 (Canceled).

26. (Original) The method of claim 16, further comprising saving a failing address for the processor.

27. (Original) The method of claim 16, further comprising saving a failing data value for the processor.

28. (Original) The method of claim 16, further comprising discontinuing an active test until the processor reads a failing address and a memory address location.

29. (Original) The method of claim 16, further comprising reporting an asynchronous interrupt to the processor.

30. (Currently Amended) A machine-readable storage medium tangibly embodying a sequence of instructions executable by ~~the~~ a machine to perform a method comprising:

~~transmitting an initiation signal from a processor via a bus to a first memory testing engine coupled with a first application specific integrate circuit via a first bus slave controller; and~~

~~testing a first random access memory associated with the first integrated circuit using the first memory testing engine~~accessing a memory associated with an application specific integrated circuit (ASIC) via a utility bus slave (UBS) controller over a bus;

configuring a memory test engine (MTE) by writing to the UBS controller over said bus; and

processing a signal from the MTE that a test of said memory is complete.

31. (Currently Amended) The machine-readable storage medium of claim 30, further comprising instructions that when executed by the machine cause:

~~transmitting an initiation signal from the processor via the bus to a plurality of memory testing engines, each coupled with a application specific integrate circuit via a bus slave controller~~ accessing a plurality of memories associated with a plurality of ASICs via a plurality of UBS controllers over the bus;

configuring a plurality of MTEs over said bus; and

~~testing a random access memory associated with the integrated circuit using the memory testing engine~~processing a plurality of signals from the MTEs that tests of said memories are complete.

Claims 32-33 (Canceled).

34. (Currently Amended) The machine-readable storage medium of claim ~~33~~31, further comprising instructions that when executed control the capturing and comparing of an actual random access memory response to the test data.

35. (Currently Amended) The machine-readable storage medium of claim 30, wherein the instructions are such that the testing comprises writing multiple data patterns per ~~a~~ memory location within the ~~first random access~~ memory and comparing a reading of the location with an expected response.

36. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~testing memory in an incrementing memory address order~~instructions that when executed configure the MTE by writing to a register controller.

37. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~testing~~ instructions that when executed test memory in a decrementing memory address order.

Claims 38-39 (Canceled).

40. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~saving~~ instructions that when executed save a failing address for the processor.

41. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~saving~~ instructions that when executed save a failing data value for the processor.

42. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~discontinuing~~ instructions that when executed discontinue an active test until ~~the~~ a processor reads a failing address and a memory address location.

43. (Currently Amended) The machine-readable storage medium of claim 30, further comprising ~~reporting~~ instructions that when executed report an asynchronous interrupt to ~~the~~ a processor.

a3

44. (Currently Amended) An apparatus comprising:

~~a~~ means for ~~transmitting an initiation signal from a processor via a bus to a first memory testing engine coupled with a first application specific integrate circuit via a first bus slave controllers~~simultaneously testing each of a plurality of memories;

means for initiating the testing; and

~~a~~ means for ~~testing a first random access memory associated with the first integrated circuit using the first memory testing engine~~giving the initiation means access to each of the plurality of memories and access to the testing means.

Claims 45-46 (Canceled).

47. (Original) The apparatus of claim 44, further comprising a means for generating test data and expected responses.

48. (Original) The apparatus of claim 47, further comprising a means for capturing and comparing an actual random access memory response to the test data.

Claims 49-53 (Canceled).

54. (Currently Amended) The apparatus of claim 44, further comprising a means for saving a failing address for the ~~processor~~initiation means.

55. (Currently Amended) The apparatus of claim 44, further comprising a means for saving a failing data value for the ~~processor~~initiation means.

a3

56. (Currently Amended) The apparatus of claim 44, further comprising a means for discontinuing an active test until the ~~processor~~ initiation means reads a failing address and a memory address location.

57. (Currently Amended) The apparatus of claim 44, further comprising a means for reporting an asynchronous interrupt to the ~~processor~~initiation means.